REMARKS

Applicant has withdrawn the pending application from Appeal and filed a Request for Continued Examination. This communication is responsive to the Advisory Action mailed September 23, 2005. In this Amendment, Applicant has amended claims 1, 2, 9, 18, 24, 30, 34 and 35. Claims 1-9, 11-32, 34-35 remain pending.

Claim Rejection Under 35 U.S.C. § 103

In the Final Office Action, the Examiner rejected claims 1-9, 11-32, 34-35 under 35 U.S.C. 103(a) as being unpatentable over Mathur (USPN 6,424,658) in view of Muller et al. (USPN 6,245,680).

Applicants have amended the claims to direct the claims to embodiments in which at least one control unit buffers data communicated between two network interfaces differently based on the direction the data flows relative to the bandwidths of the network interfaces. As one example, Applicant's amended claim 1 now explicitly requires at least one control unit that determines a direction of communication for the data between the first network interface and the second network interface. As amended, claim 1 requires that the control unit buffer the data using the embedded memory internal to the integrated circuit when the data is communicated from the first interface having the lower bandwidth to the second interface having the higher bandwidth. Claim 1 also requires that the control unit buffers the data in the external memory when the data is communicated from the second interface having the higher bandwidth to the first interface having the lower bandwidth.

As another example, claim 30 is directed to a method and, as amended, requires accessing a forwarding table with a control unit of the network router to determine a network destination for the data. Amended claim 30 further requires, when the destination requires forwarding the data to a second routing component internal to the router using a switch having a higher bandwidth than the network interface, buffering the inbound data within an embedded memory internal to the first routing component. In addition, amended claim 30 requires, when the destination requires forwarding the outbound data to the network interface having a lower bandwidth than the switch, buffering the outbound data within a memory external to the first routing component.

Support for the amendment can be found throughout the present application. As one example, the present application describes exemplary operation of the routing components as follows:

> *The mode of operation illustrated in FIG. 3 may be employed to communicate packets from switch fabric 16 to WAN interface 14, or vice versa. For example, to communicate a packet from switch fabric 16 to WAN interface 14, routing component 12A first receives the packet from switch fabric 16.* ***Because switch fabric 16 has a higher bandwidth than WAN interface 14, routing component 12A uses external memory device 30 to store the packet.*** *Routing component 12A then transmits the packet via WAN interface 14.*
>
> *To communicate a packet from WAN interface 14 to switch fabric 16, on the other hand, routing component 12A receives the packet from WAN interface 14.* ***Because switch fabric 16 has a higher bandwidth than WAN interface 14, routing component 12A uses embedded memory device 34 to store the packet.*** *Next, routing component 12A selects an interface to transmit the packet to switch fabric 16 and outputs the packet using the selected interface.*[1]

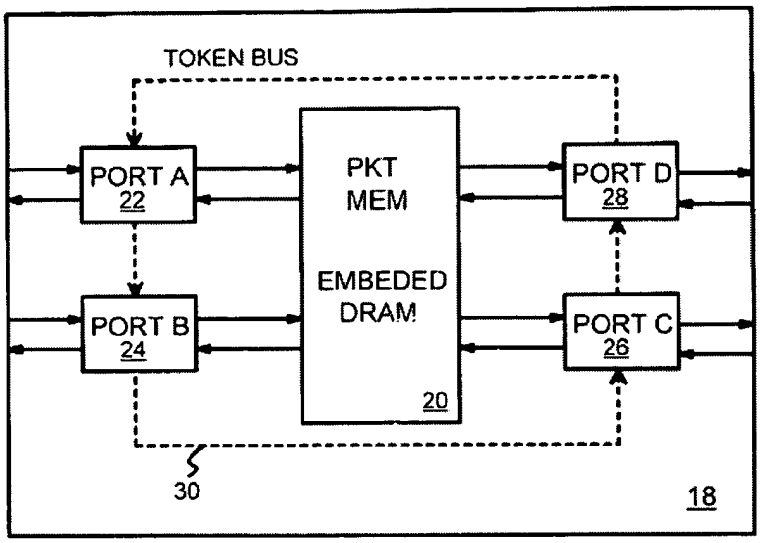
Applicant respectfully traverses the rejection to the extent applicable to the amended claims. The applied references fail to disclose or suggest the inventions defined by Applicant's claims, and provide no teaching that would have suggested the desirability of modification to arrive at the claimed invention. Before addressing the individual claim rejections, Applicant provides a brief summary of the prior art.

Mathur (USPN 6,424,658)

Mathur describes a store-and-forward network switch that uses an embedded dynamic-random-access memory (DRAM) packet memory. In particular, FIG. 2 of Mathur shows a network switch chip 18 that receives packets from one of four ports A, B, C, D and stores the packets in embedded DRAM packet memory 20. The network switch chip 18 transmits the

[1] Pg. 9, ll. 9-17 (emphasis added).

stored packets out to one or more of the four ports A, B, C, D. The following illustrates FIG. 2 of Mathur:



Mathur makes clear that packets forwarded in any direction between ports 22-28 are stored in embedded packet memory 20. For example, at col. 6, ll. 3-7, Mathur specifically states the following:

> *Port logic 22, 24, 26, 28 are bi-directional ports to a network node connected to a computer, peripheral, LAN segment, or other network equipment such as another switch, router, repeater, bridge or hub. Packets may be input or output from any port. When a packet is received by port logic 22, 24, 26, 28, it first writes the packet into embedded DRAM packet memory 20.*

Thus, as stated above and illustrated in FIG. 2 (above), Mathur teaches a switch in which packets forwarded between any of the four interface ports 22-26 are buffered within an embedded packet memory 20 regardless of the forwarding direction and without taking into account the bandwidth differences between the interfaces.

Muller et al. (USPN 6,246,680)

Muller describes a highly integrated multi-layer switch element. According to Muller, the switch element includes multiple ports for transmitting and receiving packets over a network. FIG. 2 of Muller illustrates the described switch element:

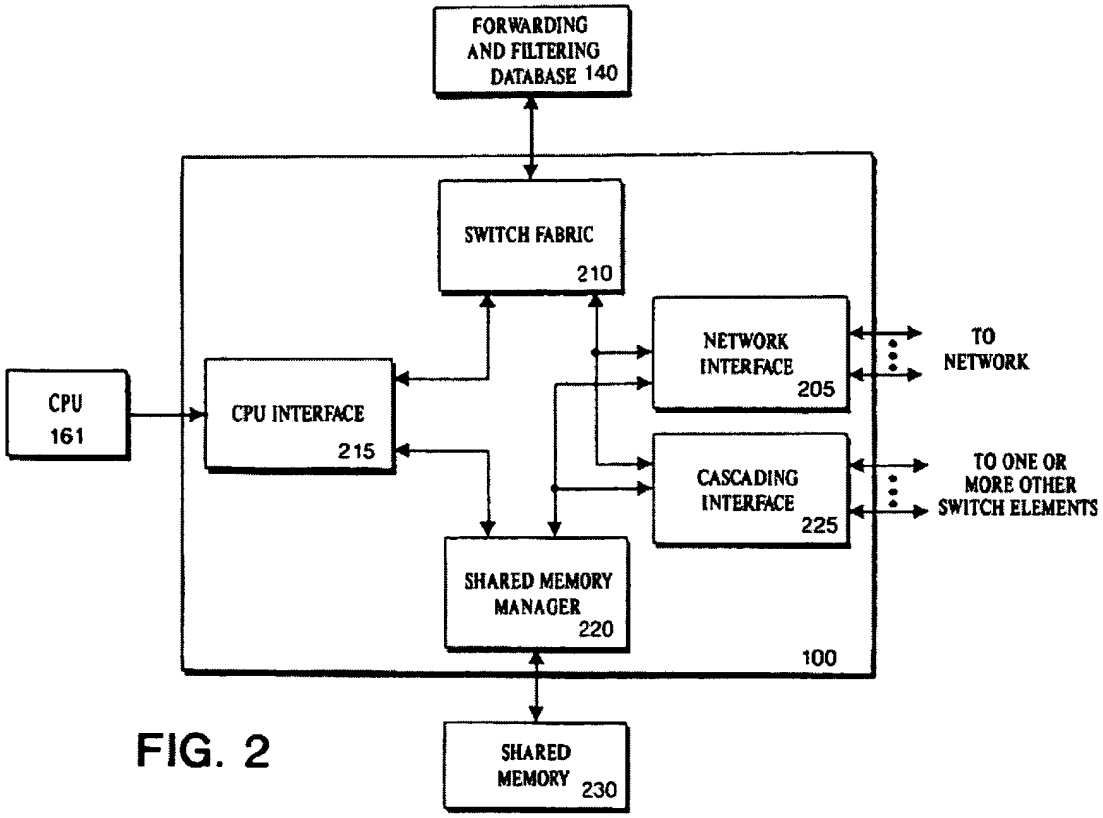


FIG. 2

Unlike Mathur, Muller makes use of an external shared memory 230 for buffering packets flowing between any of the network interfaces 205. For example, col. 1, ll. 41-60 of Muller states:

> *Input packet processing includes the following: (1) receiving and verifying incoming Ethernet packets, (2) modifying packet headers when appropriate, (3) requesting buffer pointers from the shared memory manager 220 for storage of incoming packets, (4) requesting forwarding decisions from the switch fabric block 210, (5)* ***transferring the incoming packet data to the shared memory manager 220 for temporary storage in an external shared memory 230****, and (5) upon receipt of a forwarding decision, forwarding the buffer pointer(s) to the output port(s) indicated by the forwarding decision. Output packet processing may be performed by one or more output ports of the network interface 205. Output processing includes* ***requesting packet data from the shared memory manager 220****, transmitting packets onto the network, and requesting deallocation of buffer(s) after packets have been transmitted.*

Thus, Muller teaches a switch in which an external shared memory 230 is used to buffer packets flowing in between network interfaces 205 regardless of direction and without taking into account the bandwidth differences between the interfaces.

Claims 1-9, 11-33, 34-35

Neither Mathur nor Muller, either singularly or in combination, teach or suggest a routing component having a controller that determines a direction of data communicated between a first network interface and a second network interface having different bandwidths, as required by amended claim 1. In fact, neither Mathur nor Muller describes any mechanism that determines whether data is flowing from a lower bandwidth interface to a higher bandwidth interface or vice versa. Neither reference teaches or suggests considering the relative bandwidths of both the interface from which data is being received and the interface to which data is being sent when buffering the data. As described above, Mathur specifically teaches the use of an embedded memory for buffering all data regardless of direction. Muller teaches use of a shared memory for buffering data regardless of direction. Thus, none of the prior art of record teaches or suggests a control unit or other mechanism that makes such a determination.

Moreover, none of the prior art teaches a control unit or other mechanism that actively switches the buffering scheme for data flowing between two interfaces based on the whether data is flowing from a lower bandwidth interface to a higher bandwidth interface or vice versa. Again, the prior art teaches using the same buffering technique regardless of direction. The cited art does not teach or suggest a control unit that: (1) buffers the data using the embedded memory internal to the integrated circuit when the data is communicated in a first direction from the first interface having the lower bandwidth to the second interface having the higher bandwidth, and then (2) buffers the data in the external memory when the data is communicated in a second direction from the second interface having the higher bandwidth to the first interface having the lower bandwidth.

In part, the Examiner rejects claim 1 as obvious by arguing that Muller teaches "providing buffering that is proportional to the amount of traffic through a given port."[2] For support, the Examiner relies on col. 8, ll. 35-40. In this regard the Examiner is in part correct in

[2]Advisory Action, pg. 2 and Office Action dated 5/31/05 at pg. 3.

that Muller refers to a dynamic memory allocation scheme. In other words, Muller describes dynamic allocation of "chunks" of memory space within a fixed memory address range to a port based on the amount of traffic handled by that port. Specifically, Muller is merely stating that memory allocation within the external shared memory is dynamic and based on the amount of traffic through a given port. In summary, Muller appears to be describing changing the amount of memory used by each port based on traffic levels.

However, contrary to the Examiner's conclusion, this does not provide a teaching or suggestion of actively switching between external and internal memories based on the relative bandwidths of both interfaces. Modification of Mathur in view of the teaching of Muller, as suggested by the Examiner, would merely lead to the modifying the device in Mathur to dynamically allocate memory space within the embedded memories based on traffic levels. Neither Mathur nor Muller teach or suggest switching between an external memory and an internal memory based on the relative bandwidths of both network interfaces, i.e., the network interface from which the data was received relative to the network interface to which the data is to be forwarded. For at least the above reasons, withdrawal of the rejection is requested.

CONCLUSION

All claims in this application are in condition for allowance. Applicant respectfully requests reconsideration and prompt allowance of all pending claims. Please charge any additional fees or credit any overpayment to deposit account number 50-1778. The Examiner is invited to telephone the below-signed attorney to discuss this application.

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